What Is Claimed Is:

1. An integrated circuit comprising:

a closed loop amplifier circuit containing an operational amplifier with a finite gain; and

a correction circuit correcting an error in an output of said closed loop amplifier, wherein said error is caused by using said operational amplifier with said finite gain, whereby said output corrected by said error approximately equals an output generated by using an ideal operational amplifier with infinite gain.

2. The integrated circuit of claim 1, wherein said finite gain is low such that said integrated circuit operates to provide a high throughput performance, and wherein said correction circuit reduces said error caused by use of said operational amplifier with low finite gain.

3. The integrated circuit of claim 1, wherein said correction circuit comprises a feedback impedance and an reference impedance of a first ratio, wherein said first ratio is determined by adjusting a desired amplification factor according to said error.

4. The integrated circuit of claim 3, wherein said first ratio equals ((F-1) (1+factor)), wherein F equals the desired amplification factor for said closed loop amplifier circuit and said factor equals ((1/A1 + 1/A2) x (1 + Z1/Z2) / 2), wherein said finite gain varies between A1 and A2.

5. The integrated circuit of claim 1, wherein said closed loop amplifier circuit receives an analog input signal and generates an analog output signal as said output, said integrated circuit further comprising:

an analog to digital converter (ADC) converting a sample of said analog output signal to an intermediate digital code,

wherein said correction circuit corrects said error by performing a mathematical operation on said intermediate digital code to generate a corrected digital code representing said output corrected for said error.

6. The integrated circuit of claim 5, wherein said intermediate digital code comprises a plurality of sub-codes (V1, V2, ... Vn) generated by a corresponding plurality of sub-ADCs contained in said ADC, wherein said closed loop amplifier circuit is contained in a first stage generating said V1, said mathematical operation comprises:

multiplying a value formed by (V2, .. Vn) by (1+Factor), wherein Factor equals (F/A), A equals sad finite gain.

7. The integrated circuit of claim 1, wherein said correction circuit divides said output by (1 - 1/A), wherein A equals said finite gain, to correct said error.

8. An analog to digital converter (ADC) converting a sample of an analog signal to a digital code, said ADC comprising:

a plurality of stages, each of said plurality of stages generating a corresponding one of a plurality of sub-codes, each of said plurality of sub-codes containing at least one bit,

wherein said sub-codes are used to generate said digital code, at least one of said plurality of stages comprising:

a sub-ADC receiving an input signal and generating a corresponding one of said plurality of sub-codes representing a strength of said input signal;

a digital to analog converter (DAC) converting said corresponding one of said plurality of sub-codes to a corresponding intermediate signal;

an subtractor subtracting said corresponding intermediate signal from said input signal to generate an subtractor output; and

a closed loop amplifier containing an operational amplifier with a finite gain, said closed loop amplifier amplifying said subtractor output to generate said input signal for a next stage; and

a correction circuit correcting an error in an output of said closed loop amplifier, wherein said error is caused by using said operational amplifier with said finite gain, whereby said output corrected by said error approximately equals an output generated by using an ideal operational amplifier with infinite gain.

9. The ADC of claim 8, wherein said finite gain is low such that said ADC operates to provide a high throughput performance, and wherein said correction circuit reduces said error caused by use of said operational amplifier with low finite gain.

10. The ADC of claim 9, wherein said finite gain is smaller than at least 6 x (N-1), wherein N represents a number of bits contained in said digital code.

11. The ADC of claim 9, wherein said correction circuit comprises a feedback impedance and an reference impedance having impedance of a first ratio, wherein said first ratio is determined by adjusting a desired amplification factor according to said error.

12. The ADC of claim 11, wherein said first ratio equals ((F-1) (1+factor)), wherein F equals the desired amplification factor for said closed loop amplifier circuit and said factor equals ((1/A1 + 1/A2) x (1 + Z1/Z2) / 2), wherein said finite gain varies between A1 and A2.

13. The ADC of claim 8, wherein said closed loop amplifier circuit receives an analog input signal and generates an analog output signal as said output, said ADC further comprising:

an analog to digital converter (ADC) converting a sample of said analog output signal to an intermediate digital code,

wherein said correction circuit corrects said error by performing a mathematical operation using said intermediate digital code to generate a corrected digital code representing said output corrected for said error.

14. The ADC of claim 13, wherein said intermediate digital code comprises a plurality of sub-codes (V1, V2, ... Vn) generated by a corresponding plurality of sub-ADCs, wherein said closed loop amplifier circuit is contained in a first stage generating said V1, said mathematical operation comprises:

multiplying a value formed by (V2, .. Vn) by (1+Factor).

15. The ADC of claim 8, wherein said correction circuit divides said output by (1 - 1/A), wherein A equals said finite gain, to correct said error.

16. The ADC of claim 8, wherein said sub-ADC comprises a flash ADC.

17. An analog to digital converter (ADC) converting a sample of an analog signal to a digital code, said ADC comprising:

a plurality of stages, each of said plurality of stages generating a corresponding one of a plurality of sub-codes, each of said plurality of sub-codes containing at least one bit, at least one of said plurality of stages comprising:

a sub-ADC receiving an input signal and generating a corresponding one of said plurality of sub-codes representing a strength of said input signal;

a digital to analog converter (DAC) converting said corresponding one of said plurality of sub-codes to a corresponding intermediate signal;

an subtractor subtracting said corresponding intermediate signal from said input signal to generate an subtractor output; and

a closed loop amplifier containing an operational amplifier with a finite gain, said closed loop amplifier amplifying said subtractor output to generate said input signal for a next stage; and

a correction circuit receiving said plurality of sub-codes and performing a mathematical operation on said plurality of sub-codes to generate said digital code, said mathematical operation being designed to correct an error present in said input signal generated by said closed loop amplifier due to the use of said operational amplifier with said

finite gain.

18. The ADC of claim 17, wherein said finite gain is low such that said ADC operates to provide a high throughput performance, and wherein said correction circuit reduces said error caused by use of said operational amplifier with low finite gain.

19. The ADC of claim 18, wherein said finite gain is smaller than at least 6 x (N-1), wherein N represents a number of bits contained in said digital code.

20. The ADC of claim 17, wherein said intermediate digital code comprises a plurality of sub-codes (V1, V2, ... Vn) generated by a corresponding plurality of sub-ADCs including said sub-ADC, wherein said closed loop amplifier circuit is contained in a first stage generating said V1, said mathematical operation comprises:

multiplying a value formed by (V2, .. Vn) by (1+Factor).

21. The ADC of claim 17, wherein said correction circuit divides said output by (1 - 1/A) to correct said error, wherein A equals said finite gain.

22. The ADC of claim 17, wherein said sub-ADC comprises a flash ADC.

23. A device comprising:

an analog to digital converter (ADC) converting a sample of an analog signal to a digital code, said ADC comprising:

a plurality of stages, each of said plurality of stages generating a corresponding one of a plurality of sub-codes, each of said plurality of sub-codes containing at least one bit, at least one of said plurality of stages comprising:

a sub-ADC receiving an input signal and generating a corresponding one of said plurality of sub-codes representing a strength of said input signal;

a digital to analog converter (DAC) converting said corresponding one of said plurality of sub-codes to a corresponding intermediate signal;

an subtractor subtracting said corresponding intermediate signal from said input signal to generate an subtractor output; and

a closed loop amplifier containing an operational amplifier with a finite gain, said closed loop amplifier amplifying said subtractor output to generate said input signal for a next stage;

a correction circuit correcting an error in an output of said closed loop amplifier, wherein said error is caused by using said operational amplifier with said finite gain, whereby said output corrected by said error approximately equals an output generated by using an ideal operational amplifier with infinite gain; and

a processing block processing said digital code.

24. The device of claim 23, wherein said finite gain is low such that said ADC operates to provide a high throughput performance, and wherein said correction circuit reduces said error caused by use of said operational amplifier with low finite gain.

25. The device of claim 23, wherein said finite gain is smaller than at least 6 x (N-1),

wherein N represents a number of bits contained in said digital code.

26. The device of claim 24, wherein said correction circuit comprises a feedback impedance and an reference impedance having resistance of a first ratio, wherein said first ratio is determined by adjusting a desired amplification factor according to said error.

27. The device of claim 26, wherein said first ratio equals ((F-1) (1+factor)), wherein F equals the desired amplification factor for said closed loop amplifier circuit and said factor equals ((1/A1 + 1/A2) x (1 + Z1/Z2) / 2), wherein said finite gain varies between A1 and A2.

28. The device of claim 23, wherein said closed loop amplifier circuit receives an analog input signal and generates an analog output signal as said output, said ADC further comprising:

an analog to digital converter (ADC) converting a sample of said analog output signal to an intermediate digital code,

wherein said correction circuit corrects said error by performing a mathematical operation using said intermediate digital code to generate a corrected digital code representing said output corrected for said error.

29. The device of claim 28, wherein said intermediate digital code comprises a plurality of sub-codes (V1, V2, ... Vn) generated by a corresponding plurality of sub-ADCs, wherein said closed loop amplifier circuit is contained in a first stage generating said V1, said mathematical operation comprises:

multiplying a value formed by (V2, .. Vn) by (1+Factor).

30. The device of claim 23, wherein said correction circuit divides said output by (1 - 1/A) to correct said error, wherein A equals said finite gain.

31. The device of claim 23, wherein said device comprises a wireless base station.